30nm and 20nm Physical Gate Length CMOS Transistors
(Invited Paper)

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I. Introduction

CMOS transistors with 30nm and 20nm physical gate lengths are required for the 65nm and 45nm logic technology nodes respectively. These transistors will be operating at supply voltages (Vcc) of less than a volt for low power operation. We have fabricated high-performance 30nm physical gate length CMOS transistors using conventional process flow and equipment modules. These transistors show excellent short channel effect and Ion/Ioff characteristics at Vcc = 0.85V [1], and they will be ready for production in 2005. We have also been conducting research on the 20nm physical gate length CMOS for the 45nm logic technology node, and have successfully demonstrated functional 20nm transistors with healthy IV characteristics. In this paper we review the 30nm CMOS transistor results [1], discuss the importance of Vcc scaling, and also give a preview on the 20nm transistor research results.

II. 30nm CMOS Transistor Results [Ref. 1]

A TEM cross section of the 30nm transistor is shown in Fig. 1. The I_d-V_g characteristics of the 30nm NMOS transistor are shown in Fig. 2. The CMOS transistors achieve NMOS gate delay (CV/I) of 0.85 ps as shown in Fig. 3, and PMOS gate delay of 1.7 ps as shown in Fig. 4, at Vcc=0.85V. These are the smallest CV/I values ever reported for integrated Si CMOS devices. The results show that conventional planar CMOS transistors are scalable to the 65nm logic technology node, with excellent short channel effect and device performance at 30nm physical gate length and Vcc = 0.85V.

III. Importance of Supply Voltage Scaling

The choice of sub-1.0V supply voltage is important for the 65nm logic technology node and beyond for low power operation. To illustrate the importance of low Vcc, we compare the energy-delay product (C^2V^3/I) of the 30nm NMOS transistor operating at 0.85V and a high-performance 35nm NMOS transistor operating at 1.5V. The fabrication of the 35nm transistors was similar to that of the 30nm transistors, but it was optimized for high Vcc operation. Fig. 5 shows the I_d-V_g characteristics of the 35nm NMOS (Idsat = 1.1mA/um, Ioff = 50nA/um at Vcc = 1.5V). Fig. 6 shows the comparison results. The data show that the 35nm NMOS at 1.5V has 3.7 times higher energy-delay product than the 30nm NMOS at 0.85V for similar gate delay, and that the latter is much more suitable for the 65nm logic technology node for low power and high speed applications.

IV. Preview on the 20nm Transistor

We have been conducting research on the 20nm physical gate length transistors for the 45nm logic technology node, and have successfully demonstrated functional 20nm transistors with healthy IV characteristics. Fig. 7 shows a TEM cross section of the 20nm transistor. Compared to the 30nm transistor which has polySi electrode height of 60nm, the 20nm transistor has polySi electrode height of 40nm. The Id-Vd curves of a 20nm NMOS transistor are shown in Fig. 8.

V. Summary

High-performance 30nm physical gate length CMOS transistors operating at Vcc = 0.85V have been demonstrated for the 65nm logic technology node, which will be ready for production in 2005. Research on the 20nm physical gate length transistors is being conducted for the 45nm logic technology node.

VI. Reference

1. R. Chau et al, *IEDM Technical Digest*, p.45-48, 2000.

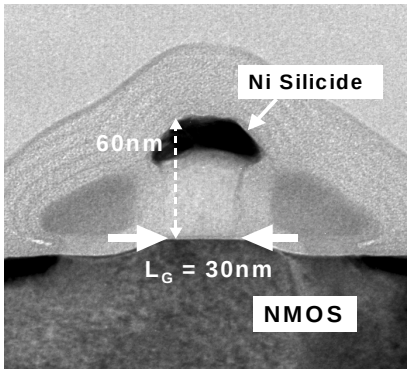

Fig. 1. TEM cross section of the 30nm transistor.

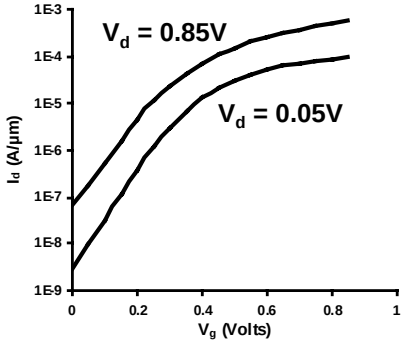

Fig. 2. Id-Vg characteristics of the 30nm NMOS transistor.

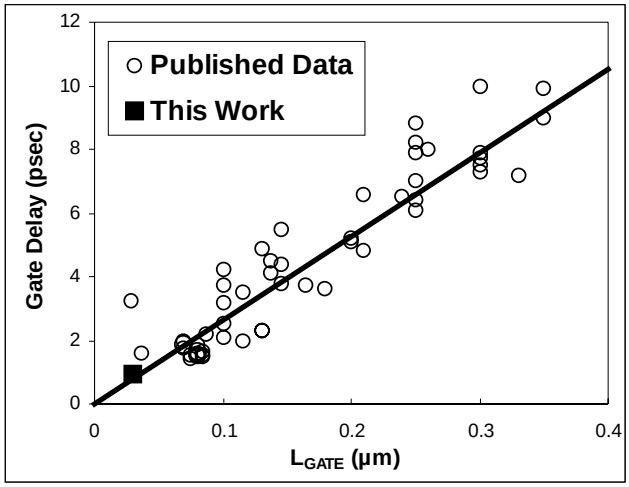

Fig. 3. NMOS gate delay vs physical gate length trend.

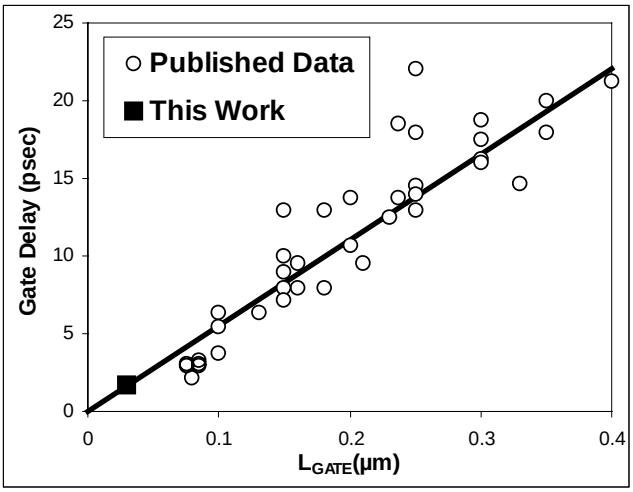

Fig. 4. PMOS gate delay vs physical gate length trend.

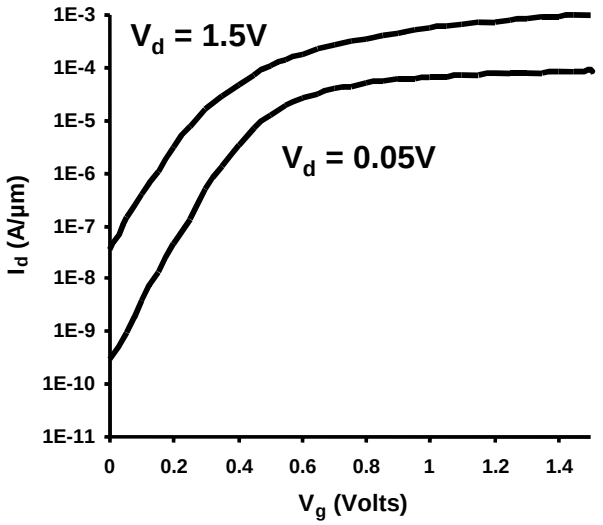

Fig. 5. Id-Vg characteristics of a 35nm NMOS transistor.

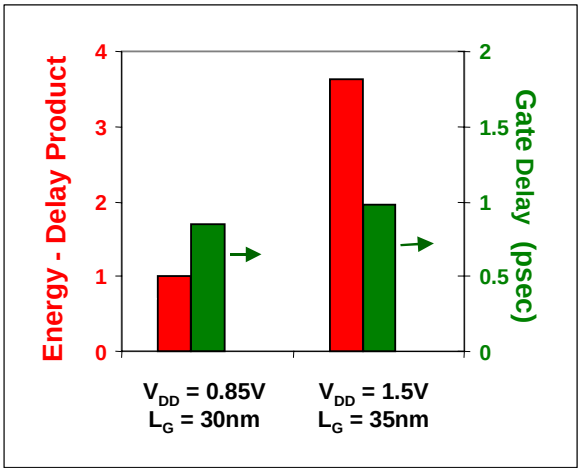

Fig. 6. Energy-delay product and CV/I gate delay of the 30nm NMOS at 0.85V versus the 35nm NMOS at 1.5V.

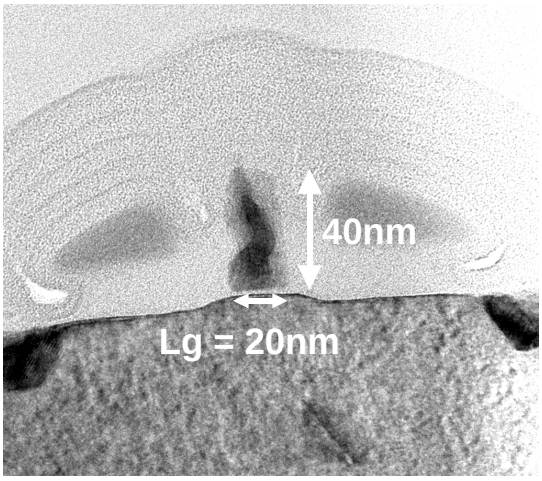

Fig. 7. TEM cross section of a 20nm NMOS transistor.

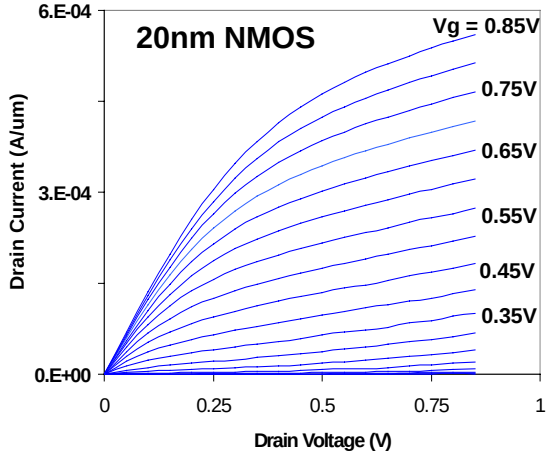

Fig. 8. Id-Vd characteristics of the 20nm NMOS transistor.